Flash Magic Application Note 1

ISP Entry using COM Port Handshaking Signals

EMBEDDED SYSTEMS ACADEMY

1. Introduction

Flash Magic can control the entry into ISP mode of some Philips devices by using the COM Port handshaking signals to control the device. Typically the handshaking signals are used to control such pins as Reset, PSEN and VCC. The exact pins used depend on the specific device.

When this feature is supported, Flash Magic will automatically place the device into ISP mode at the beginning of an ISP operation. Flash Magic will then automatically cause the device to execute code at the end of the ISP operation.

To support this feature in your hardware, a specific circuit must be used. The circuit varies depending on the device.

This application note describes the circuit required and the waveforms expected.

2. P89C51Rx2Hxx, P89C66x, P89C51Rx2xx, P89C6xX2

2.1 Circuit

The following is a simplified circuit diagram. Note that the reset circuit is a suggestion only, and may be modified to suit the application.

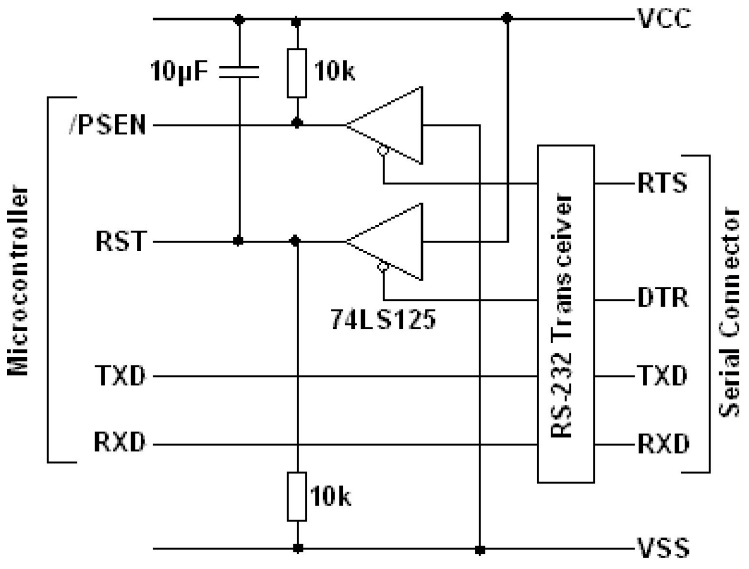

Figure 1 – Example Simplified Circuit Diagram

When the COM port is closed, RTS and DTR are at a RS232 voltage level below –3V. This converts to TTL logic level 1, ensuring that the tristate gates are turned off and therefore their outputs are floating. The tristates have no effect on the normal operation of the RST and /PSEN pins and so RST is connected

to a reset circuit, for example using a capacitor and resistor and /PSEN is weakly pulled high, allowing the device to control /PSEN to access external memory.

When a serial cable is not connected, the RS232 inputs of the RS232 transceiver are pulled low, generating TTL logic 1 at the outputs. This ensures the tristate gates are turned off.

When the COM port is opened and a serial cable is connected, Flash Magic may set DTR or RTS to a voltage level above +3V to generate TTL logic 0 on the RS232 transceiver outputs. When the DTR output is TTL logic 0, RST is pulled high, placing the device in reset. When the RTS output is TTL logic 0, /PSEN is pulled low, required for ISP entry.

2.2 Flash Magic Options

By checking the option to assert RTS while the COM Port is open in Flash Magic, the RTS TTL signal output from the RS232 transceiver will remain at logic 0 while the ISP operation is performed. This allows hardware to be designed that can reset or reconfigure hardware for an ISP operation.

T1 and T2 are timing values for the waveforms Flash Magic generates with the DTR and RTS signals. Entering values in milliseconds into Flash Magic may configure these timings. Note however that the timings are approximate as they depend on what other applications are running in Windows and how fast the PC is.

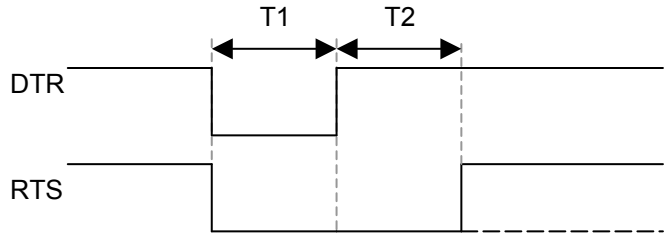

Figure 2 – Timing of DTR and RTS TTL Signals (outputs of RS232 transceiver) at Start of ISP Operation

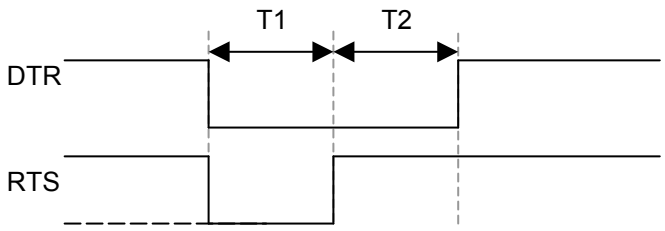

Figure 3 – Timing of DTR and RTS TTL Signals (outputs of RS232 transceiver) at End of ISP Operation

2.3 Waveforms

The following are the expected waveforms when performing an ISP operation (read of security bits, programming, blank check, etc). The waveforms are taken from various points in the circuit. Note that the timing depends on the values entered for T1 and T2 into Flash Magic. Also the length of time to complete the ISP operation may vary depending on the crystal frequency. A 20MHz crystal was used with a P89C51RD2Hxx to generate these waveforms. The ISP operation used to generate these waveforms was reading the security bits.

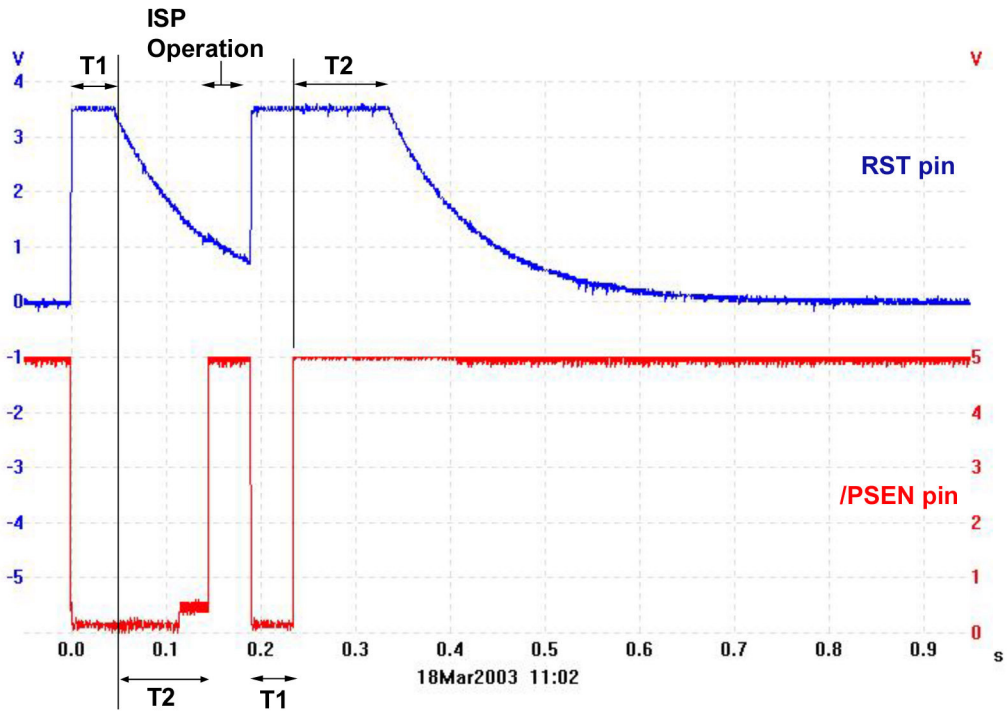

Figure 4 – TTL Waveforms at RST and /PSEN pins

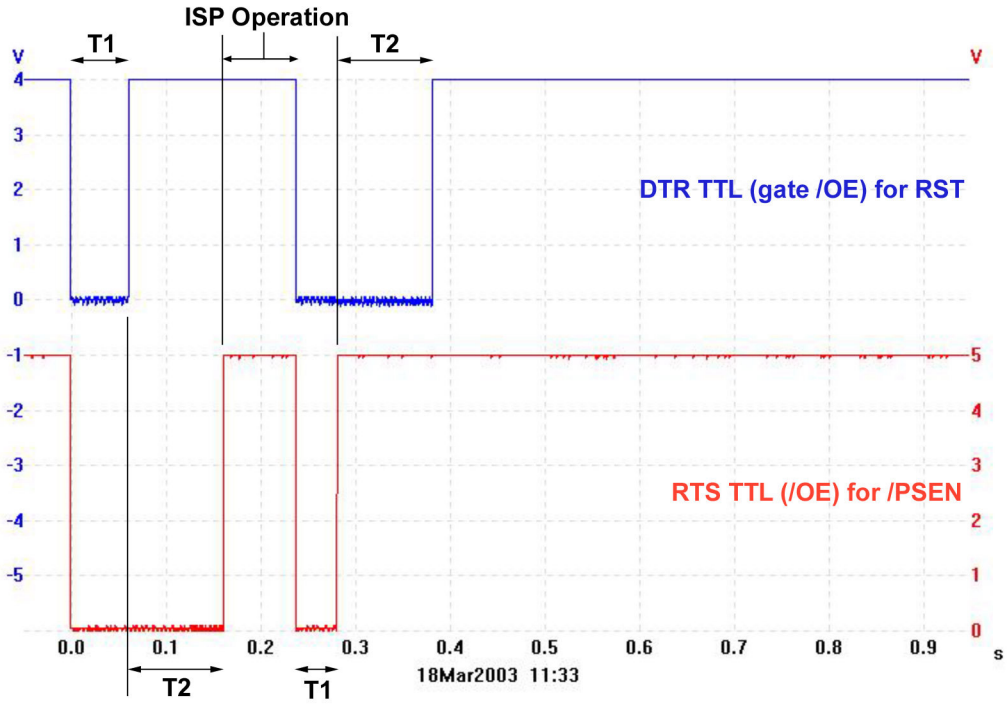

Figure 5 – TTL Waveforms at /OE controls of tristates (outputs of RS232 transceiver)

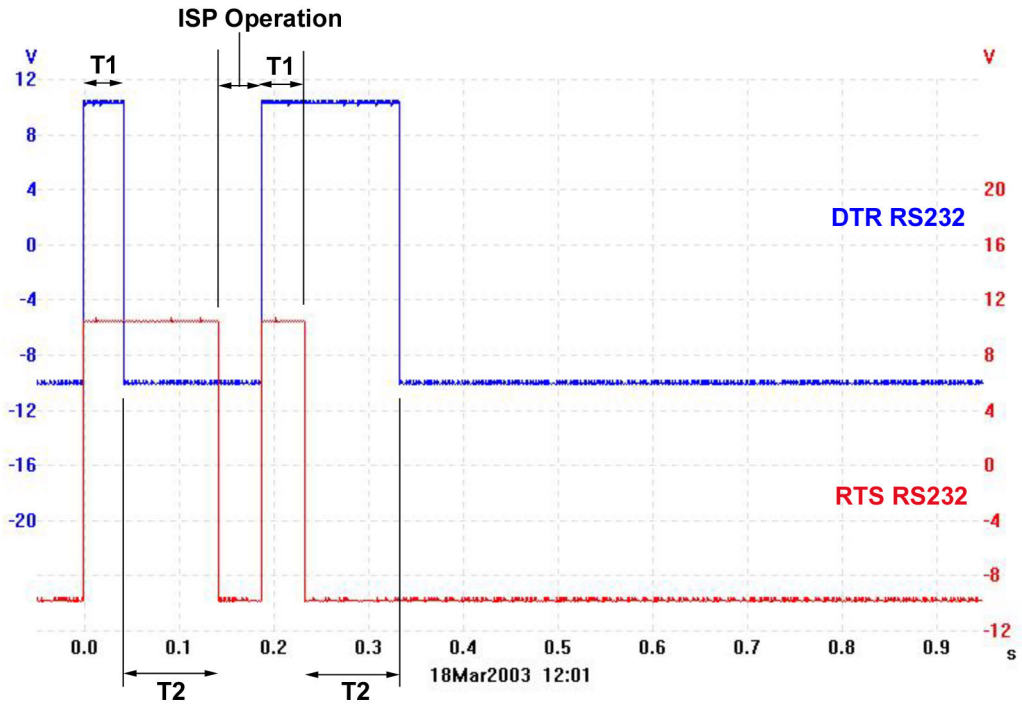

Figure 6 – RS232 Waveforms on Serial Cable

3. P89LPC932

3.1 Circuit

Keil Software designed the following circuit and it is currently the only circuit supported by Flash Magic to place the LPC932 into ISP mode using the COM Port handshaking signals. The circuit is implemented on Keil Software's MCB900 board.

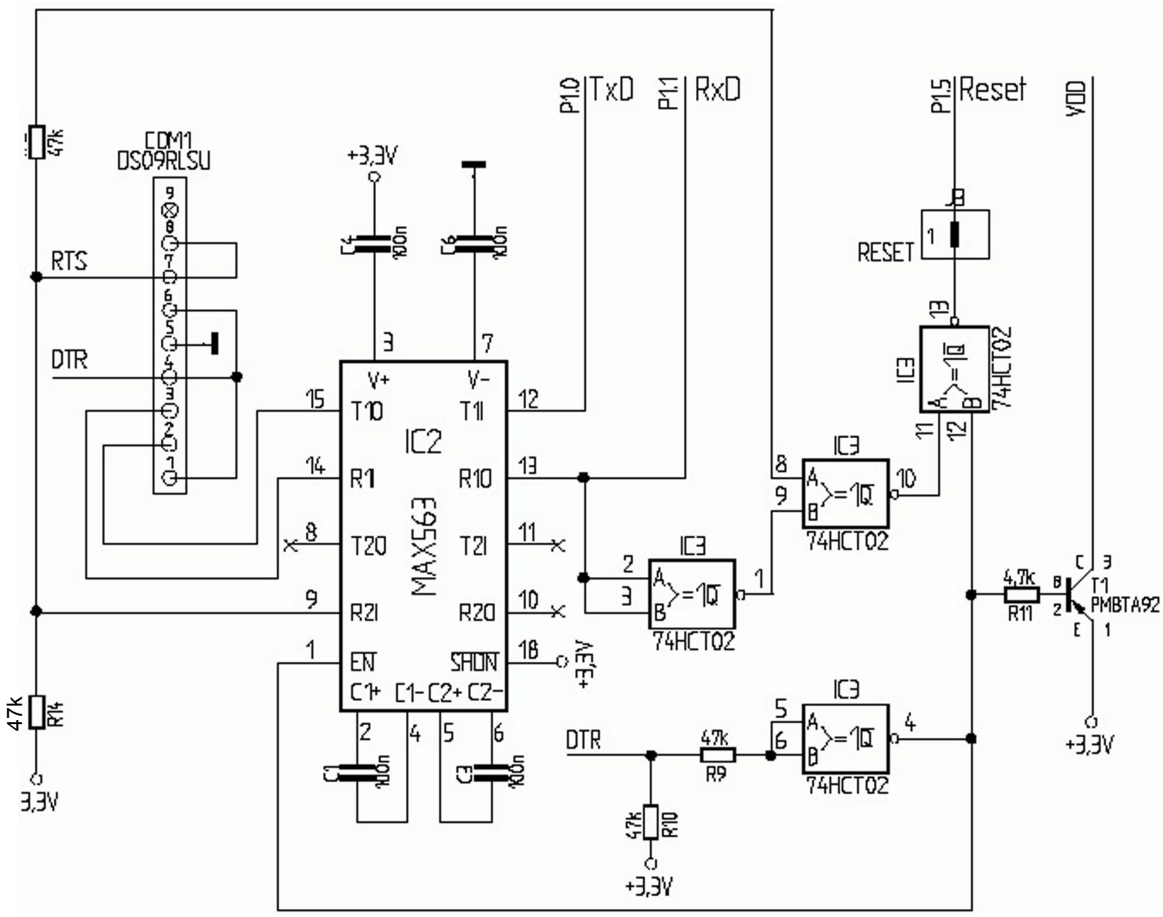

Figure 7 – 89LPC932 ISP Circuit Schematic Diagram

Resistors R9 and R10 clamp the voltage of DTR to TTL voltage levels. The output of IC3 at pin 4 is the inverse of DTR, resulting in the output producing logic 0 when DTR is asserted, and a logic 1 when DTR is not asserted. Asserting DTR therefore switches on transistor T1 providing power to the device on pin VDD. When DTR is not asserted, power is not applied to the device.

Resistors R13 and R14 clamp the voltage of RTS to TTL voltage levels resulting in a logic 0 when RTS is not asserted and a logic 1 when RTS is asserted. The output of IC3 at pin 1 is the inverse of RxD, i.e. /RxD. Therefore the output of IC3 at pin 10 is RxD when RTS is not asserted, and 0 when RTS is asserted. When the device is powered up (i.e. IC3 pin 12 is 0), the /Reset pin is the inverse of IC3 pin 11. Therefore /RST is at logic 1 if RTS is not asserted, otherwise if RTS is asserted it is at /RxD.

So, when DTR is asserted the device is powered up. When DTR is not asserted the device is powered down. When the device is powered up, asserting RTS causes /RxD to be connected to the /RST pin, otherwise the /RST pin is at 1, allowing code to execute.

3.2 Waveforms

The following are the expected waveforms when performing an ISP operation (read of security bits, programming, blank check, etc). The waveforms are taken from various points in the circuit. Note that the length of time to complete the ISP operation may vary depending on the crystal frequency. The internal 7.3728MHz oscillator was used when generating these waveforms. The ISP operation used to generate these waveforms was reading the security bits.

The first waveform – figure 8 – shows the signals on the device VDD and /RST pins for an entire ISP operation from beginning to end. The remaining waveforms show a close-up of the start of the ISP operation, and all use the same time base.

Before the device is reset into ISP mode, Flash Magic configures the COM Port. During this process the COM Port is opened and closed, producing pulses on DTR, RTS and RxD.

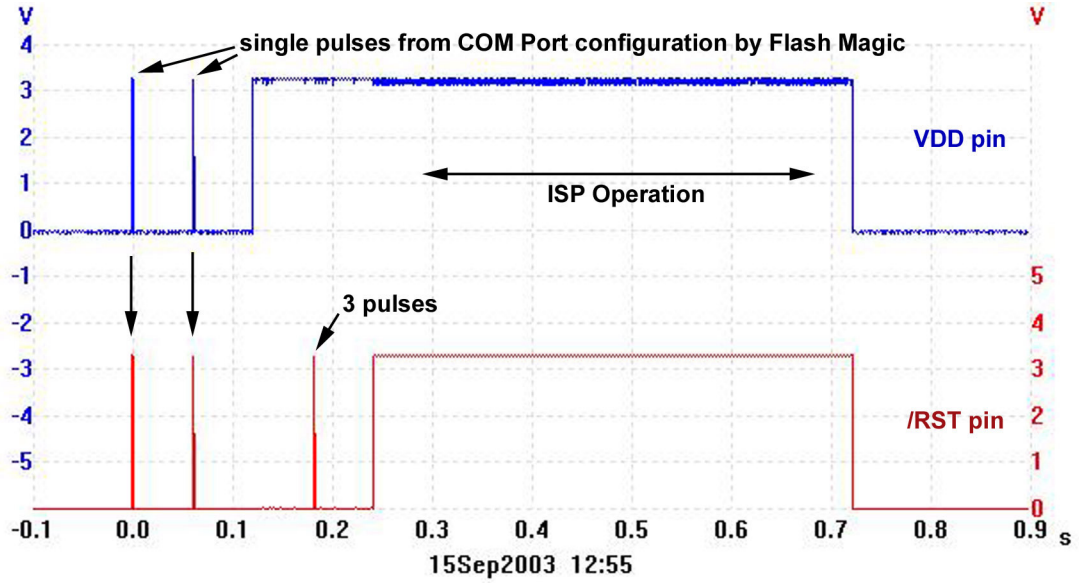

Figure 8 – TTL waveforms on the VDD and /RST pins for an entire ISP operation

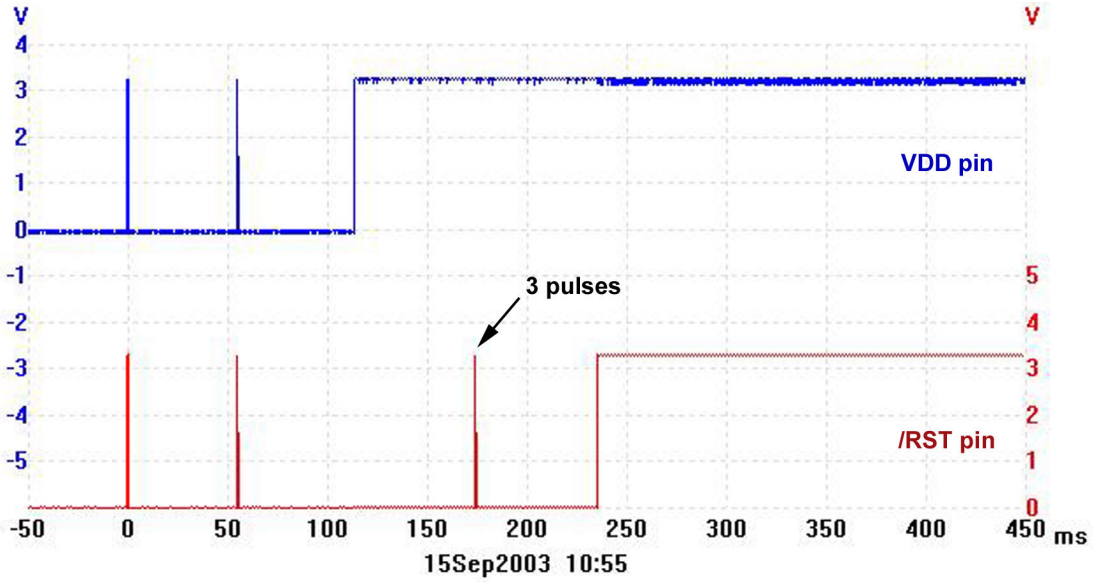

Figure 9 – TTL waveforms for VDD and /RST pins

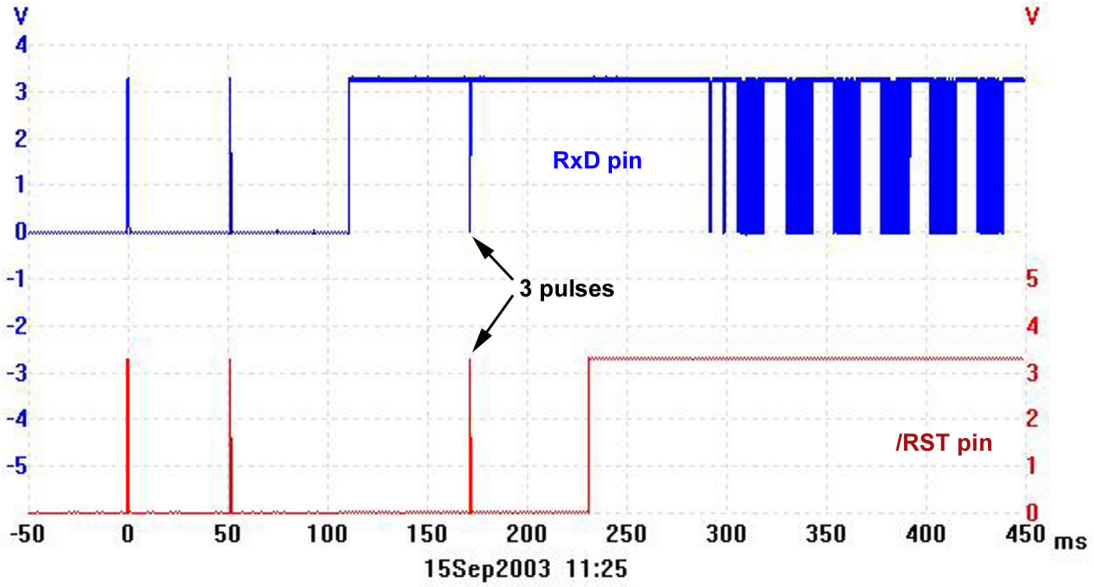

Figure 10 – TTL waveforms for RxD and /RST pins

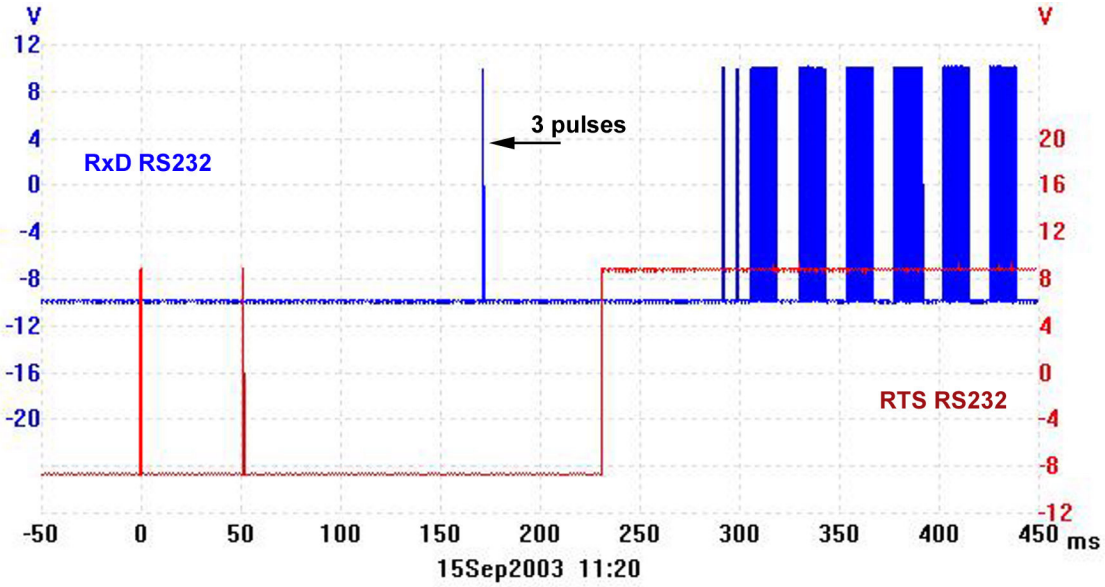

Figure 11 – RxD and RTS waveforms on the serial cable

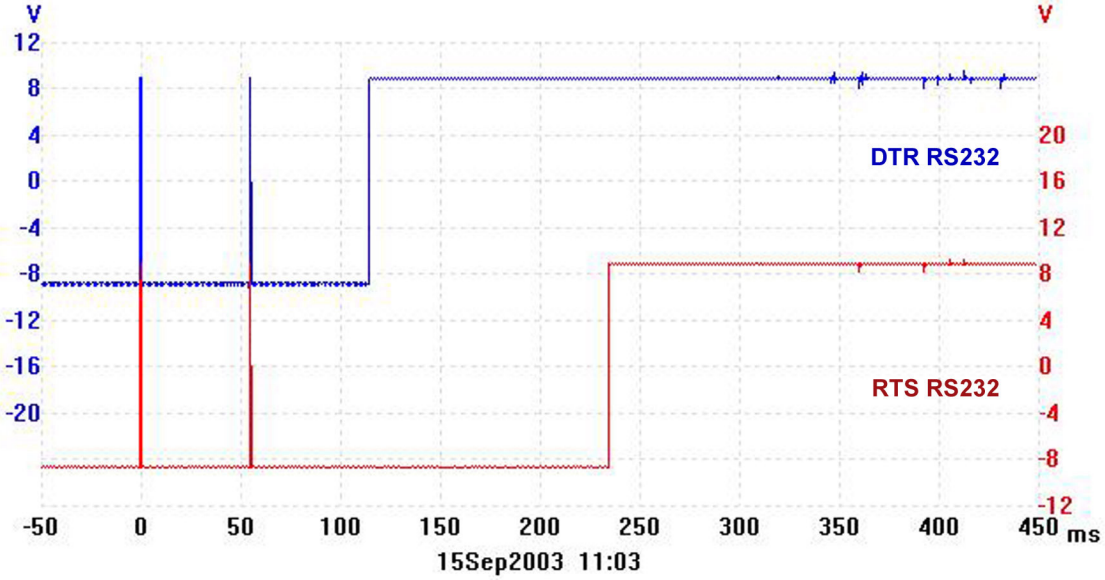

Figure 12 – DTR and RTS waveforms on the serial cable